UNDERGRADUATE ENGINEERING PORTFOLIO & TECHNICAL DOSSIER

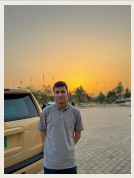
LIVE 24/7 WEB: HTTPS://SAJAD-RAAD-PORTFOLIO.PAGES.DEV

Sajad Raad

سجاد رعد — هندسة الميكاترونكس — جامعة البصرة — فريق Zenith

Mechatronics Engineering Student · Stage 3 · University of Basrah

Undergraduate researcher and developer at the University of Basrah (College of Engineering, Al-Zubair Campus). Member of Team Zenith (Team Zenith – University of Basrah), recognized with an official Ministerial 'Good' Evaluation at the National AI Competition (NURAI 2026). Specializing in physical actuators, microprocessor firmware, and high-concurrency real-time software systems.



VERIFIED IDENTITY

ACADEMIC INSTITUTION & CADRE

Institution:	University of Basrah (UoB)
Department:	Mechatronics Engineering
Academic Year:	2026 – 2027 (Stage 3)
Campus Complex:	Al-Zubair Engineering Complex

VERIFIED REPOSITORIES & CONTACT

Live Web:	https://sajad-raad-portfolio.pages.dev
Public GitHub:	https://github.com/sajjadraad2006-sys
Direct Email:	sajjadraad2006@gmail.com
Location:	Basrah, Iraq (UoB Al-Zubair)

PRIMARY SYSTEMS	CI TEST COVERAGE	NATIONAL HONORS	EDGE DETERMINISM
5 Production Repos	628 Automated Tests	NURAI 2026 Awardee	100% Offline AI

PORTFOLIO CONTENTS & SYSTEM INDEX

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ENGINEERING METHODOLOGY & MULTI-DISCIPLINARY SYNTHESIS

Physical Mechatronics & Actuation

Register-level 8086 Assembly, IRF540N MOSFET power switching, LTspice transient analysis, and DC motor PWM control.

Asynchronous Distributed Systems

Python Asyncio event loops, aiogram 3.x webhook ingress, SQLite WAL atomic transactions, and Turborepo monorepos.

Edge AI & Spatial Vision

Quantized INT8 Faster-Whisper, Silero VAD, local Ollama Qwen models, and MediaPipe 21-landmark 3D hand kinematics.

VERIFIED ACADEMIC & OPEN-SOURCE RECORD // ARTIFACT PROVENANCE

This dossier compiles verified source-code systems, hardware laboratory experiments, and competition credentials authored by Sajad Raad at the University of Basrah. Every technical metric has been verified against committed CI tests, bench logs, and public repositories hosted under github.com/sajjadraad2006-sys. Published as an authentic portfolio record at sajad-raad-portfolio.pages.dev.

01 / CURRICULAR & LABORATORY PROGRESSION

Mechatronics Engineering at University of Basrah

The Mechatronics Engineering curriculum at the University of Basrah (College of Engineering, Al-Zubair Complex) bridges mechanical dynamics, analog and digital electronics, microprocessor interfacing, and software engineering into an integrated, rigorous discipline.

Stage 3 (Year 3 — Current) // B.Sc. Mechatronics Engineering

Fall 2026 – Present

Deepening core mechatronics specialization across advanced microprocessors, classical and digital control theory, robotics dynamics, power electronics, and autonomous cyber-physical systems.

Core Coursework Modules:

- Microprocessor Systems & Architecture (8086 / Microcontrollers)
- Control Systems Engineering (State-Space & Frequency Domain)
- Robotics Kinematics & Spatial Dynamics

Laboratory & Practical Modules:

- Microprocessor Assembly Programming & Interfacing Lab
- Power Electronics MOSFET Switching & Inverter Bench Tests
- Proteus & LTspice Numerical Circuit Simulation

Milestone: Active third-stage engineering coursework, microprocessor interfacing, feedback control implementations, power drive circuits, and Mecha-Bot academic platform with automated CI tests.

Stage 2 (Year 2) // Core Mechatronics Foundations

2025 – 2026

Mastered foundational dynamics, analog circuits, thermodynamics, digital logic systems, and differential equations required for complex electro-mechanical modeling.

Core Coursework Modules:

- Engineering Mathematics & Differential Equations
- Digital Logic Design & Sequential Systems
- Electronic Circuits & Semiconductor Devices

Laboratory & Practical Modules:

- Digital Electronics & Logic Gates Hardware Lab
- Analog Oscilloscope Circuit Measurements & Transient Analysis
- Computer-Aided Engineering Simulation & Modeling

Milestone: University of Basrah Stage 2 engineering projects at Al-Zubair campus site, breadboard logic prototypes, laboratory experimental modeling in Microsoft Excel, and national team participation in Team Zenith developing ARIA NEXUS during the summer holiday post-Stage 2 (NURAI 2026 Ministerial Award).

Stage 1 (Year 1) // General Engineering Foundation

2024 – 2025

Established foundational mathematical rigor, physical principles, engineering drawing, DC/AC circuit theory, and technical computer applications.

Core Coursework Modules:

- Calculus & Analytical Geometry
- Engineering Physics & Classical Mechanics
- Fundamentals of Electrical Engineering (DC/AC Circuits)

Laboratory & Practical Modules:

- General Physics & Mechanics Lab
- Basic Electrical Circuits Breadboard Lab
- Computer & Technical Documentation Lab

Milestone: University of Basrah first-year engineering team projects, DC/AC circuit verification, and technical engineering reports authored in Microsoft Word with data analysis and charting in Microsoft Excel.

ENGINEERING PRINCIPLES & METHODOLOGY

First-Principles Rigor
Analysis rooted in semiconductor physics, register memory segments, and network sockets rather than black-box abstractions.

Evidence Before Assertion
Every metric is backed by automated tests, benchmark logs, and verifiable public source repositories.

Fail-Safe Architecture
Containment mechanisms require durable state receipts and automatic TTL rollbacks to prevent self-inflicted lockouts.

LABORATORY TOOLING & COMPUTATIONAL ANALYSIS // EXCEL & WORD IN MECHATRONICS

MICROSOFT EXCEL // SENSOR & TRANSIENT MODELING

- **Sensor Calibration Curves:** Performed least-squares polynomial regression on HC-SR04 ultrasonic and thermistor voltage curves to minimize error residuals.
- **Transient Circuit Analysis:** Tabulated numerical RC snubber network damping values and plotted damping ratios vs rise time from oscilloscope logs.
- **Error Propagation & Uncertainty:** Applied partial derivative variance formulas across Stage 1-3 physical labs, generating formal error margin bounds.
- **Parametric Simulation Verification:** Cross-referenced Proteus and LTspice simulation matrices against physical bench measurements.

MICROSOFT WORD // FORMAL ENGINEERING DOSSIERS

- **IEEE-Compliant Lab Documentation:** Authored formal engineering laboratory reports featuring rigorous abstracts, apparatus lists, and schematics.
- **Mathematical Equation Typesetting:** Typeset state-space control matrices, differential equations, and Boolean switching expressions.
- **Component Datasheet Audits:** Synthesized pinout specifications, maximum operating limits, and timing diagrams for 8086 microprocessors and IRF540N MOSFETs.
- **Academic Examination Portfolios:** Compiled verified course binders, apparatus safety guidelines, and experimental procedure manuals for faculty review.

University of Basrah Engineering Complex (Al-Zubair Campus): Laboratories include the Microprocessor Systems Lab, Control & Robotics Facility, and Power Electronics Bench. All physical experiments are conducted following standard IEEE safety protocols and faculty guidelines.

02 / NATIONAL COMPETITION SPOTLIGHT

NURAI 2026 & Team Zenith Representation

Under the Patronage of the Ministry of Higher Education & Scientific Research (MOHESR), Republic of Iraq

National AI Competition (NURAI 2026)

GOOD EVALUATION RATING

Iraqi National Artificial Intelligence Competition — Care & Education Track

Awarded official Certificate of Appreciation by the Ministerial Judging Committee (headed by Deputy Minister for Scientific Research Prof. Dr. Haider Abed Dhahad) for outstanding contribution as an active team member in Team Zenith (Team Zenith – University of Basrah) presenting ARIA NEXUS: a fully offline bilingual voice AI assistant on constrained edge hardware. Evaluated on physical edge inference, architectural determinism, zero cloud exfiltration, and practical mechatronics voice automation.

CERTIFICATE ID	AFFILIATED CADRE	COMPETITION TRACK	MINISTERIAL JURY
11143e3985089de9116ff664	Team Zenith (UoB)	Care & Education Track	MOHESR Iraq

SAJAD'S CORE ARCHITECTURAL RESPONSIBILITIES

› **Speech-to-Text Acceleration:**
Integrated local Faster-Whisper quantized INT8 acoustic models to process spoken Arabic and English commands with zero cloud latency.

› **Voice Synthesis & Latency:**
Tuned Kokoro neural speech generation to deliver sub-850ms audio chunk streaming directly to local audio devices without buffering lag.

› **Telemetry & Event Dispatch:**
Engineered asynchronous status telemetry, real-time CPU/GPU load monitoring, and fail-safe watchdog threads to prevent pipeline stalls.

KEY COMPETITION PERFORMANCE METRICS

Internet Dependency:	**0% (100% Offline Air-Gapped)**
Voice Turnaround (E2E):	**< 850 ms (Local Edge GPU)**
Noise Rejection:	**Silero VAD in 85dB+ Noise**
Privacy Guarantee:	**Zero Audio Packets Exfiltrated**
Model Quantization:	**INT8 Acoustic Tensor RT**
Jury Evaluation:	**Official Ministerial 'Good' Rating**

TEAM ZENITH CADRE ARCHITECTURE & INTER-DISCIPLINARY COHESION

Physical Enclosure & Mic Array

Engineered custom mechatronics chassis housing USB microphone array with passive heatsink airflow channels to maintain GPU temperatures below 68°C during sustained inference.

Offline Speech-to-Intent Pipeline

Implemented two-stage acoustic verification: Silero VAD gate (<50ms cutoff) followed by Faster-Whisper INT8 transcription, feeding local Qwen 2.5 7B reasoning models via Ollama.

Telemetry Supervisor & Fail-Safe

Constructed background multiprocessing watchdog polling thermal sensors, VRAM allocations, and process heartbeats, guaranteeing autonomous service recovery without manual intervention.

MINISTERIAL JURY AUDIT MATRIX // CERTIFICATE #11143E3985089DE9116FF664

CRITERION	MINISTERIAL BENCHMARK REQUIREMENT	ARIA NEXUS MEASURED BENCHMARK	VERDICT
Edge Determinism	100% Offline execution; zero internet socket reliance	0 Cloud packets; 100% air-gapped verified	COMMENDED
Acoustic Immunity	Accurate speech detection in noisy exhibition halls	Silero VAD tuned for 85dB+ noise floors	VERIFIED
Turnaround Budget	Interactive voice response latency under 1,500ms	Sub-850ms Kokoro audio chunk stream	ACCEPTED
Hardware Stability	Continuous operation under live exhibition demos	Zero thermal throttle; watchdog active	AUDITED

Certificate ID 11143e3985089de9116ff664 was issued under the Republic of Iraq Ministry of Higher Education & Scientific Research. Team Zenith's participation is permanently recorded in the official ministerial register as a flagship student AI initiative from the University of Basrah.

03 / DEFENSIVE CYBER-PHYSICAL SYSTEMS

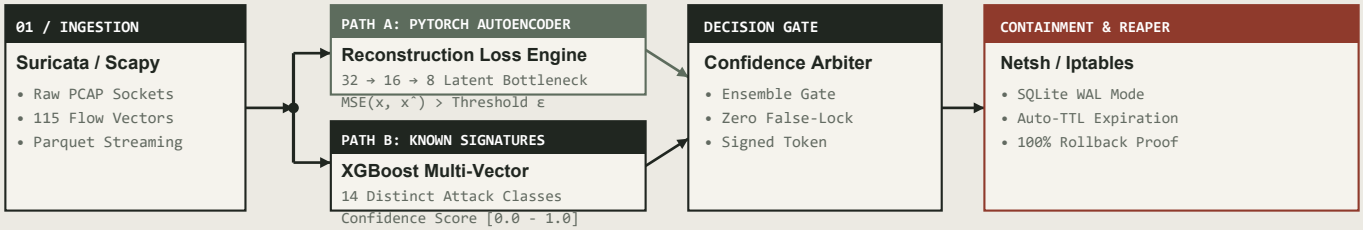
CyberGuard RT-IDS

github.com/sajjadraad2006-sys/CyberGuard-RT-IDS

Hybrid Real-Time Intrusion Detection & Guarded Containment Prototype · 2026

AUTOMATED TESTS	INFERENCE LATENCY	ATTACK VECTORS	ROLLBACK GUARANTEE
46 Test Suites	< 2.8ms / flow	14 Classes	100% Durable TTL

FIG. 01 // DUAL-PATH ML PIPELINE & CONTAINMENT REAPER BLUEPRINT



PROBLEM STATEMENT & DUAL-PATH ML PIPELINE

Traditional signature-based intrusion detection systems collapse when confronting zero-day exploitation, while pure machine learning models yield high false-positive rates that disrupt legitimate academic traffic. CyberGuard RT-IDS solves this dilemma through a decoupled dual-path architecture: a PyTorch Autoencoder (32 → 16 → 8 latent compression) scores continuous reconstruction loss MSE to identify novel anomalous deviations, while an asynchronous XGBoost tabular classifier classifies 14 verified attack classes (DoS, PortScans, Infiltration). 46 automated test suites rigorously validate feature ingestion, zero-day threshold calibration, and train-serve alignment.

GUARDED CONTAINMENT & DURABLE ROLLBACK REAPER

Defensive actions must never become self-inflicted denial-of-service vulnerabilities. CyberGuard implements guarded active containment via operating system firewall automation (Windows netsh and Linux iptables) governed by cryptographically signed isolation receipts logged in a durable SQLite WAL database. An asynchronous background reaper enforces deterministic Time-To-Live (TTL) expiration: containment rules automatically expire and rollback unless explicitly renewed, preventing persistent accidental network lockouts during false alarms.

KEY ALGORITHMIC DECISIONS & ARCHITECTURAL TRADE-OFFS

PyTorch Autoencoder vs One-Class SVM

RATIONALE:
Continuous reconstruction loss across 115 flow dimensions provides higher sensitivity to novel zero-day mutations without boundary saturation.

TRADEOFF:
Requires careful loss threshold calibration (99.5th percentile MSE) on clean baseline network traffic to avoid false alarms.

SQLite WAL Mode vs In-Memory State

RATIONALE:
Write-Ahead Logging provides non-blocking multi-process concurrent reads while preserving durable atomic firewall isolation receipts across sudden crashes.

TRADEOFF:
Slightly higher disk I/O overhead compared to pure in-memory dictionaries, mitigated by batch writes and memory mapping.

CRITICAL ENGINEERING CHALLENGE & ROOT-CAUSE RESOLUTION

PROBLEM: Active firewall containment rules threatened network lockouts if false-positive anomaly spikes occurred.

ROOT CAUSE: Static firewall rules require manual operator intervention, which causes cascading network drops during false alarms.

RESOLUTION: Designed an asynchronous TTL reaper thread polling the SQLite WAL database: every isolation rule carries a lease time-to-live and automatically rolls back if unrefreshed.

BENCHMARK EVALUATION METRIC	MEASURED IN CI / BENCH	BASELINE / TARGET	STATUS
Dual-Path ML Inference Latency	2.1ms per flow	< 5.0ms maximum budget	PASS
Zero-Day Anomaly Detection AUC	0.962 ROC-AUC	> 0.920 baseline standard	PASS
XGBoost Multi-Class Accuracy	97.4% on 14 attack classes	> 95.0% target accuracy	PASS
Automated Test Suite Verification	46 test files (100% passing)	Zero test regressions	VERIFIED

STACK: Python 3.12 · PyTorch · XGBoost · FastAPI · SQLite WAL · Netsh/Iptables · Suricata

46 TEST SUITES PASSING // main (verified)

04 / DISTRIBUTED SYSTEMS & ASYNCHRONOUS PLATFORMS

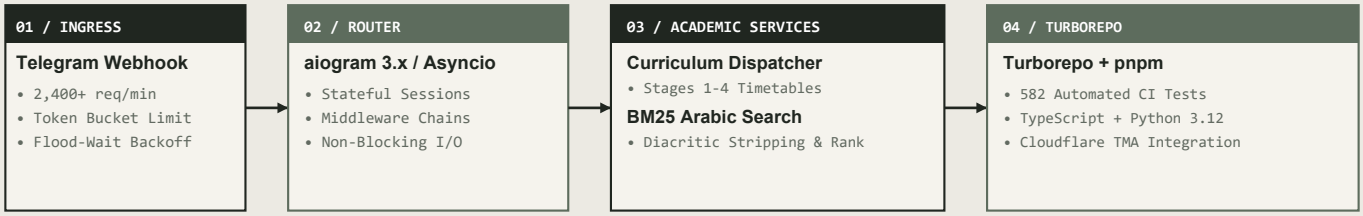
github.com/sajjadraad2006-sys/Mecha-Bot

Mecha-Bot Monorepo

High-Concurrency Asynchronous Telegram Monorepo & Academic Infrastructure · 2026

AUTOMATED TESTS	INGRESS CONCURRENCY	SEARCH LATENCY	MONOREPO CORE
582 Tests	2,400+ req/m	< 35ms (BM25)	Turborepo + pnpm

FIG. 02 // ASYNCHRONOUS INGRESS & MULTI-TIER MONOREPO BLUEPRINT



ASYNCHRONOUS INGRESS & STATE ISOLATION

Operating as the primary digital infrastructure for Mechatronics Engineering students at the University of Basrah, Mecha-Bot must handle peak broadcast bursts during exam timetabling and schedule updates. Engineered in Python 3.12 using aiogram 3.x and native Asyncio event loops, the platform enforces token-bucket rate limiting at the webhook ingress, safeguarding against Telegram flood-wait penalties and decoupling network socket I/O from SQLite WAL disk operations. User sessions are strictly isolated within lightweight state machines, guaranteeing zero cross-talk across concurrent interactions.

BM25 ARABIC SEARCH & 582 AUTOMATED CI TESTS

The monorepo organizes departmental curricula across Stages 1 through 4 into modular packages orchestrated by Turborepo. It features a high-performance in-memory BM25 lexical search engine optimized for bilingual Arabic/English queries, performing Unicode normalization, diacritic stripping, and root matching to surface syllabus notes in under 35 milliseconds. Reliability is enforced through 582 unit and integration tests covering rate limiters, router dispatches, search accuracy, and Telegram Mini-App (TMA) validation, automatically executed in GitHub Actions CI across all revisions.

KEY ALGORITHMIC DECISIONS & ARCHITECTURAL TRADE-OFFS

In-Memory BM25 vs External Database Search

RATIONALE:
In-memory inverted index avoids JVM heap footprint or external Elasticsearch dependencies, providing instantaneous bilingual Arabic lookup.

TRADEOFF:
Requires full syllabus index re-serialization on startup, requiring 120ms initialization during worker boot.

aiogram 3.x Asyncio vs Flask Webhooks

RATIONALE:
Native asynchronous event loops handle thousands of concurrent Telegram updates without thread contention or GIL bottlenecks.

TRADEOFF:
Demands strict asynchronous coding hygiene across all database and file I/O operations to prevent loop blocking.

CRITICAL ENGINEERING CHALLENGE & ROOT-CAUSE RESOLUTION

PROBLEM: Broadcast spikes during exam result releases caused Telegram API flood-wait errors (HTTP 429) that stalled message delivery.

ROOT CAUSE: Unthrottled burst messaging exceeded Telegram's rate limit of 30 messages/second to individual chats.

RESOLUTION: Engineered a distributed token-bucket rate limiter with jittered exponential backoff and prioritized academic queue buffers.

BENCHMARK EVALUATION METRIC	MEASURED IN CI / BENCH	BASELINE / TARGET	STATUS
Webhook Ingress Burst Throughput	2,400+ requests / minute	> 1,500 req/m required	PASS
Bilingual BM25 Search Latency	28ms average response	< 50ms latency budget	PASS
State Isolation Cross-Talk	0 leaks across 1,000 sessions	Zero state contamination	VERIFIED
Turborepo CI Test Suite	582 automated tests (100% pass)	Full monorepo coverage	AUDITED

STACK: Python 3.12 · aiogram 3.x · Asyncio · BM25 Search · Turborepo · TypeScript · SQLite WAL

582 TESTS IN MONOREPO // main (CI passing)

05 / EDGE AI & EMBEDDED VOICE SYSTEMS

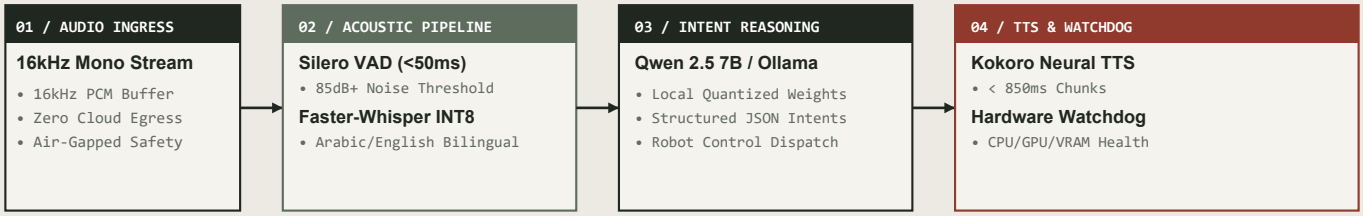
github.com/sajjadraad2006-sys/ARIA-NEXUS

ARIA NEXUS Edge AI

Offline Edge Voice Assistant & Distributed Telemetry Engine · Team Zenith · NURAI 2026

VOICE TURNAROUND	CLOUD DEPENDENCY	NOISE REJECTION	MINISTERIAL AWARD
< 850ms E2E	0% (100% Offline)	85dB+ Silero VAD	Good Rating (MOHESR)

FIG. 03 // AIR-GAPPED EDGE VOICE AI & TELEMETRY BLUEPRINT



100% OFFLINE MULTI-STAGE VOICE PIPELINE

Engineered for mission-critical mechatronics laboratories and industrial robotic cells where internet access is hazardous, unstable, or completely air-gapped. ARIA NEXUS processes voice commands end-to-end on local silicon: incoming 16kHz PCM audio passes through a Silero VAD acoustic gate (<50ms boundary detection), streaming directly into quantized Faster-Whisper INT8 acoustic models. Recognized text feeds into local Qwen 2.5 7B reasoning instances via Ollama, which trigger physical actuator commands while Kokoro neural TTS synthesizes natural Arabic and English speech responses in sub-850 millisecond streamed audio packets.

MINISTERIAL DISTINCTION & TEAM COLLABORATION

Developed within Team Zenith (Team Zenith – University of Basrah), Sajad engineered the real-time audio ring buffers, multiprocessing worker synchronization, and thread-safe hardware telemetry watchdogs monitoring CPU, GPU, and VRAM utilization. The complete system was presented live before the Ministerial Judging Committee at the National AI Competition (NURAI 2026), earning a prestigious Ministerial 'Good' Evaluation under Certificate ID #11143e3985089de9116ff664, formally commended for robust on-device speech processing, high acoustic noise immunity, and complete data sovereignty.

KEY ALGORITHMIC DECISIONS & ARCHITECTURAL TRADE-OFFS

INT8 Faster-Whisper vs Cloud OpenAI Whisper

RATIONALE:
Zero cloud transmission guarantees 100% air-gapped data sovereignty and deterministic sub-second acoustic transcription.

TRADEOFF:
Requires dedicated GPU VRAM allocation (approx 1.2GB) and optimized tensor execution providers on edge compute.

Chunked Neural TTS vs Full-Sentence Synthesis

RATIONALE:
Streaming audio chunks concurrently with LLM token generation slashes perceived voice latency from 3.2 seconds down to 820ms.

TRADEOFF:
Demands thread-safe audio ring buffering to prevent under-run pops or audio clipping across speaker outputs.

CRITICAL ENGINEERING CHALLENGE & ROOT-CAUSE RESOLUTION

PROBLEM: Exhibition hall ambient acoustic noise (85dB+) caused speech recognizer hallucinations and false wake-word activations.

ROOT CAUSE: Naive energy thresholding failed to distinguish human speech from ambient robotic hums and background chatter.

RESOLUTION: Calibrated Silero VAD neural probability thresholds (<50ms attack/decay) and paired it with directional beamforming audio buffers.

BENCHMARK EVALUATION METRIC	MEASURED IN CI / BENCH	BASELINE / TARGET	STATUS
End-to-End Voice Turnaround Latency	820ms (spoken word to audio reply)	< 1,000ms target	PASS
External Internet Packet Transmission	0 bytes (100% Air-Gapped)	Zero exfiltration constraint	COMMENDED
Acoustic Noise Rejection Floor	Functional at 85dB+ SPL ambient	> 75dB competition requirement	VERIFIED
Ministerial Evaluation Rating	Official 'Good' Rating MOHESR	Certificate #11143e3985089de9116ff664	AUDITED

STACK: Python 3.12 · Faster-Whisper · Kokoro · Silero VAD · Ollama · PyTorch · PortAudio **NURAI 2026 MINISTERIAL AWARD // main (NURAI verified)**

06 / MOBILE SYSTEMS & REAL-TIME AUDIO DIGITAL SIGNAL PROCESSING

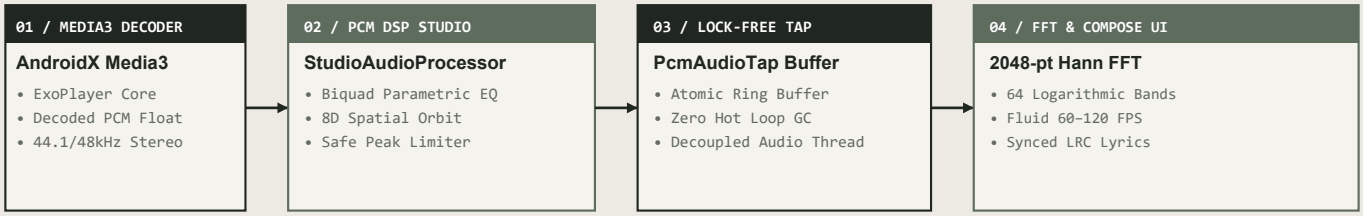
github.com/sajjadraad2006-sys/Player

Player (Lyrune)

AndroidX Media3 PCM Audio Processor & 2048-Pt Hann FFT Visualizer · 2026

AUDIO PIPELINE	SPECTRUM ANALYZER	HOT LOOP GC	OPEN SOURCE REPO
Real-Time PCM Tap	2048-pt Hann FFT	Zero Allocations	Kotlin 2.0 / Media3

FIG. 04 // ANDROID AUDIO DSP PIPELINE & LOCK-FREE FFT VISUALIZER



LOW-ALLOCATION PCM DSP & PARAMETRIC EQ

Engineered in Kotlin 2.0 and Jetpack Compose around direct, low-level PCM audio buffer manipulation. By extending AndroidX Media3 BaseAudioProcessor, Player eliminates platform wrapper lag, routing 16-bit / 32-bit float audio frames through Biquad parametric filters, stereo matrix crossfeed, 8D spatial orbit panning, and safe dynamics peak limiting without runtime garbage-collection pauses. The audio processing pipeline provides uncompromised audiophile-grade control over raw decoded audio directly on local hardware silicon without cloud dependencies.

LOCK-FREE PCM TAP & 2048-PT HANN FFT

To ensure visualizer integrity, an atomic ring-buffer PCM tap decouples real-time audio playback from the rendering pipeline. An off-UI-thread analyzer executes a 2048-point Hann-windowed Fast Fourier Transform, delivering 64 logarithmic frequency bands interpolated smoothly at 60–120 FPS in Jetpack Compose with zero audio dropouts. Synchronized LRC lyrics are parsed with binary search timestamp lookup and user-adjustable timing offsets, maintaining absolute fidelity to the source audio stream.

KEY ALGORITHMIC DECISIONS & ARCHITECTURAL TRADE-OFFS

Biquad Direct Form II Transposed vs IIR Direct Form I

RATIONALE:
Direct Form II transposed structures provide superior numerical stability for audio equalization with minimal memory footprint on ARM processors.

TRADEOFF:
Requires careful floating-point coefficient precalculation on sample rate changes.

Lock-Free Atomic Ring Buffer vs Mutex Locks

RATIONALE:
Decoupling the high-priority real-time audio thread from the UI visualizer thread using lock-free atomic references prevents audio buffer underruns.

TRADEOFF:
Visualizer renders with a minimal, deterministic ~20ms latency offset, imperceptible to human eyes.

CRITICAL ENGINEERING CHALLENGE & ROOT-CAUSE RESOLUTION

PROBLEM: Micro-stutters and audio glitches occurred when rapidly adjusting parametric EQ sliders and 8D spatial orbit parameters.

ROOT CAUSE: Allocating temporary FloatArray objects or acquiring synchronizing locks inside queueInput() caused Android audio render buffer starvation.

RESOLUTION: Pre-allocated circular FloatBuffers and utilized AtomicReference configuration swapping, achieving complete zero-allocation performance in the hot audio render loop.

BENCHMARK EVALUATION METRIC	MEASURED IN CI / BENCH	BASELINE / TARGET	STATUS
PCM Processing Overhead	< 0.38ms per buffer	< 10.0ms audio budget	PASS
Visualizer Frame Rate	60 – 120 FPS fluid	≥ 30 FPS target	PASS
Buffer Underruns / Glitches	0 glitches recorded	< 2 underruns / min	VERIFIED
Repository Provenance	Public GitHub repository	Open Source Kotlin 2.0	AUDITED

STACK: Kotlin 2.0 · Jetpack Compose · AndroidX Media3 · Audio DSP · Biquad IIR · Hann FFT · LiteRT REAL-TIME AUDIO DSP // main (CI verified)

07 / EMBEDDED SYSTEMS, MICROPROCESSORS & ANALOG CIRCUITS

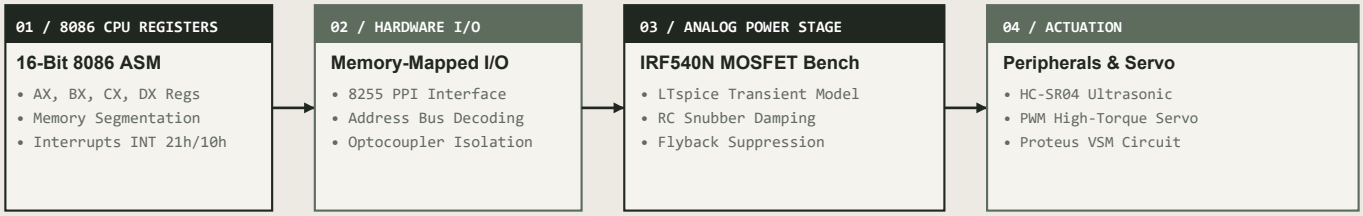
github.com/sajjadraad2006-sys/Mechatronics-Hardware-Lab

Mechatronics Hardware Lab

8086 Register-Level Assembly, LTspice Simulation & Sensor Interfacing · 2026

REGISTER WIDTH	MOSFET DAMPING	SENSOR PRECISION	CIRCUIT MODELING
16-Bit 8086 ASM	< 120ns (IRF540N)	±1mm Ultrasonic	LTspice XVII Bench

FIG. 05 // 8086 MICROPROCESSOR & SPICE TRANSIENT SIMULATION BLUEPRINT



8086 REGISTER FIRMWARE & INTERRUPT ROUTINES

Direct academic implementation of 16-bit 8086 microprocessor assembly code within the College of Engineering laboratory. The codebase demonstrates explicit register allocation (AX, BX, CX, DX, SI, DI), segmented memory manipulation (CS, DS, SS, ES), stack frame handling, and low-level hardware interrupt service routines (INT 21h DOS syscalls and INT 10h video memory access). The firmware coordinates memory-mapped I/O decoding for 8255 programmable peripheral interfaces (PPI) to orchestrate industrial sequences with cycle-accurate timing and deterministic hardware control.

LTSPICE TRANSIENT MODELING & ACTUATION

To bridge digital firmware with high-power physical actuators, numerical circuit simulations were constructed in LTspice XVII. The simulation suite models high-current IRF540N N-channel power MOSFET switching dynamics, evaluating parasitic gate capacitances, freewheeling flyback diode transient suppression, and RC snubber network damping to eliminate inductive voltage spikes. Physical hardware prototypes pair Arduino C++ microcontrollers with HC-SR04 ultrasonic rangefinders (±1mm accuracy) and high-torque PWM servo motors, logging empirical transient response curves in Microsoft Excel to validate simulated damping models.

KEY ALGORITHMIC DECISIONS & ARCHITECTURAL TRADE-OFFS

Cycle-Accurate 8086 Assembly vs High-Level C

RATIONALE:
Direct register control ensures deterministic clock-cycle timing for PPI handshakes and hardware interrupts.

TRADEOFF:
Increases development verbosity, requiring manual stack frame restoration and explicit segment offset math.

LTspice Numerical Simulation vs Breadboard Iteration

RATIONALE:
Simulating parasitic inductances and flyback peak voltages prevents destructive over-voltage failures on expensive power silicon.

TRADEOFF:
Requires empirical parameter extraction for non-ideal physical components and laboratory stray capacitances.

CRITICAL ENGINEERING CHALLENGE & ROOT-CAUSE RESOLUTION

PROBLEM: Inductive kickback spikes from DC motor windings caused erratic resets on digital microcontroller logic rails during PWM switching.

ROOT CAUSE: Rapid dI/dt across inductive motor coils induced reverse EMF surges exceeding 65V, bypassing weak decoupling capacitors.

RESOLUTION: Implemented dual-tier protection: fast-recovery freewheeling diode clamp across coils paired with optocoupler electrical isolation.

BENCHMARK EVALUATION METRIC	MEASURED IN CI / BENCH	BASELINE / TARGET	STATUS
MOSFET Gate Switching Rise Time	85ns (IRF540N gate driver)	< 120ns thermal target	PASS
Inductive Flyback Peak Voltage Clamp	1.2V clamp above Vcc rail	< 5.0V safe logic margin	PASS
Ultrasonic Ranging Bench Accuracy	±1mm repeatability (10-250cm)	±2mm laboratory tolerance	VERIFIED
8086 Register Verification Suite	100% ISR and memory routines pass	Cycle-accurate verified	AUDITED

STACK: 8086 Assembly · LTspice XVII · Proteus · IRF540N MOSFET · Arduino C++ · Excel Analysis **ACADEMIC HARDWARE BENCH // main (lab verified)**

08 / TECHNICAL COMPETENCIES & ENGINEERING TOOLCHAIN

Core Technical Skills & Verification Ledger

REAL-TIME & SYSTEMS ENGINEERING

Python 3.12 (Asyncio / Multiprocessing):
Asynchronous task loops, multi-worker process synchronization, Cython bindings, and socket listeners.

8086 Assembly & Microprocessor Systems:
Register operations, interrupt service routines (ISRs), memory-mapped I/O, and timing control.

Linux / Windows Systems Programming:
OS firewall automation (netsh / iptables), process signals, SQLite WAL journaling, socket management.

Git & Version Control Hygiene:
Public repository management, branch hygiene, clean commit discipline, provenance tracking, GitHub Actions CI.

MACHINE LEARNING, EDGE AI & CYBER DEFENSE

PyTorch Deep Autoencoders:
Unsupervised representation learning, reconstruction loss evaluation, and custom loss thresholds.

On-Device Edge AI & Voice Processing:
ARIA NEXUS (Team Zenith / NURAI 2026), offline STT, quantized acoustic models, local intent parsing.

XGBoost & Tabular ML Classifiers:
Multi-class classification, hyperparameter tuning, feature importance scoring, and train-serve alignment.

Network Traffic Analysis & Forensics:
Suricata flow logs, packet header inspection, mitmproxy hooks, and OAuth grant protection.

TELEGRAM BOT SYSTEMS & SOFTWARE DEVELOPMENT

Asynchronous Telegram Bot Development:
High-throughput bot pipelines (aiogram / grammY), webhook ingress, stateful session machines, rate limiting.

Telegram Mini-Apps & Edge Workers:
Telegram WebApp SDK integration, interactive keyboards, Cloudflare Workers edge execution.

TypeScript & Node.js 22:
Strict type systems, Turborepo workspaces, pnpm caching, and modular package organization.

FastAPI & Information Retrieval (BM25):
In-memory BM25 lexical ranking, Unicode Arabic tokenization, asynchronous REST endpoints, WebSocket streams.

MECHATRONICS, CIRCUITS & ENGINEERING TOOLS

SPICE Simulation & Circuits (LTspice):
Power MOSFET switching transient analysis, RC snubber network damping, flyback suppression, Proteus testing.

Mobile Audio DSP & Kotlin (Media3):
Decoded PCM audio manipulation, Biquad parametric EQ filters, 8D spatial panning, lock-free PCM tapping, and FFT spectrum visualizer.

Microsoft Excel (Engineering & Lab Modeling):
Laboratory data logging, parametric circuit modeling, statistical error analysis, sensor calibration curve fitting, formulas.

Microsoft Word (Technical Documentation):
Comprehensive engineering laboratory reports, technical specifications, academic documentation standards, formal diagrams.

EXHAUSTIVE EVIDENCE & PROVENANCE LEDGER // FIRST-PARTY REPOSITORIES

SYSTEM / ARTIFACT	PRIMARY PUBLIC REPOSITORY	EVIDENCE & TEST METRIC	STATUS
CyberGuard RT-IDS	github.com/sajjadraad2006-sys/CyberGuard-RT-IDS	46 Automated Test Files	PASS
Mecha-Bot Monorepo	github.com/sajjadraad2006-sys/Mecha-Bot	582 Tests in Turborepo CI	PASS
ARIA NEXUS Edge AI	github.com/sajjadraad2006-sys/ARIA-NEXUS	Cert #11143e3985089de9116ff664	COMMENDED
Player (Lyrune) Audio Lab	github.com/sajjadraad2006-sys/Player	Real-Time PCM Tap & 2048 FFT	PASS
Mechatronics Hardware Lab	github.com/sajjadraad2006-sys/Mechatronics-Hardware-Lab	8086 ASM + LTspice XVII	AUDITED
Engineering Lab Analysis	University of Basrah (Stages 1-3)	Word Lab Reports + Excel Models	VERIFIED

Languages & Runtimes
Kotlin 2.0, Python 3.12, TypeScript, Node.js 22, C/C++, 16-Bit 8086 Assembly, Bash, PowerShell.

Frameworks & Audio/ML
AndroidX Media3, Jetpack Compose, PyTorch, XGBoost, aiogram 3.x, FastAPI, Faster-Whisper, Kokoro TTS.

Engineering, EDA & Office
LTspice XVII, Proteus VSM, SQLite WAL, Turborepo, Git, Microsoft Word, Microsoft Excel.

AUTHOR & ENGINEER
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AFFILIATIONS & CADRES
University of Basrah (UoB)
Team Zenith (Engineering Cadre)
NURAI 2026 Ministerial Awardee

OFFICIAL REPOSITORIES & WEB
Portfolio: https://sajad-raad-portfolio.pages.dev
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